Remarks

Claim 1 is amended. No new matter is introduced by the amendment, and entry thereof is requested.

Claims 1 - 17 and 19 - 36 are in the application, of which claims 20 - 34 were earlier withdrawn as directed to a nonelected invention. Accordingly, claims 1 - 17, 19, 35 and 36 are now under consideration.

Reconsideration of the Application, as amended, is requested.

Applicant's invention is directed to multi-package modules (MPM) including stacked first and second packages, each of which includes a die attached to a package substrate, in which the first and second package substrates are interconnected by wire bonding, and in which the first package includes a flip-chip ball grid array package having a flip-chip in a die-up configuration. Advantageously, according to the invention, the second package and the first package can be separately tested before assembly, so that second packages not testing as "good" can be discarded and only "good" second packages used in the finished MPM.

The points raised in the Office action will now be addressed.

Rejections under 35 U.S.C. § 102(b)

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Maeda JP 2001/223326 ("Maeda JP '326"). The Examiner asserted that:

> Maeda discloses in e.g., Fig. 8 and Fig. 2 a multi-package module (12) comprising
> - stacked first (1 and 3; abstract, lines 8 and 9) and second packages (2 and 4; abstract, lines 8 - 10),
> - each said package including a die (1 and 2) attached to a passive substrate (3 and 4),
> - wherein the first (3) and second (4) substrates are interconnected by wire bonding (9; abstract, line 12), and wherein the first package (1 and 3) comprises a flip-chip ball grid array package having a flip-chip (1) in a die-up configuration (see Fig. 8).

This rejection is traversed.

First, generally: Maeda JP '326 does not teach or suggest a multi-package module comprising stacked first and second packages, each said package including a die attached to a

substrate, as in Applicant's invention as claimed. Maeda JP '326 describes (referring to the Figs. and the abstract):

- (Fig. 3) providing a "tape-board";
- (Fig. 4) mounting a first die by flip-chip interconnection on the tape board and laminating a "wiring film" on the first die;
- (Fig. 5) mounting a second chip on the wiring film by flip-chip connecting;
- (Fig. 6) wire bonding connecting electrodes on the film to a connecting electrode on the board
- (Fig. 7) resin-sealing the chips, the wire, and the like;
- (Fig. 8) disposing a plurality of solder bumps on the rear surface of the board.

That is, the second die according to Maeda JP '326 is not affixed to the wiring film until after the wiring film is put onto the first chip; in other words, Maeda JP '326 does not teach or suggest providing a second package (including a chip attached to a substrate) and thereafter stacking the second package onto a first package. This distinction is significant: according to Applicant's invention the first and second packages can be tested before they are stacked, so that only packages testing as "good" are used; in the device described by Maeda JP '326, there is no testable second package.

Accordingly, Maeda does not suggest, much less teach, all the features of Applicant's invention as claimed and, accordingly, the rejection of claim 1 as being anticipated by Maeda JP '326 should be withdrawn.

Moreover, Maeda JP '326 does not teach or suggest a first package comprising a flip-chip ball grid array package having a flip-chip in a **die-up** configuration. Maeda clearly shows the first die attached to the tape board in a die-down configuration (*e.g.*, Fig. 7). Merely inverting the package (as in Maeda JP '326 Fig. 8), to which the Examiner refers, does not make a die-up package. As Applicant's specification makes clear, the die in the die-up first package according to the invention is affixed on the side of the substrate to which the second level interconnect solder balls are attached (the "lower" side, whatever the orientation of the package may be). See, for example, Applicant's paragraph [0079]:

> The bottom package of the MPM according to the invention can be a flip chip package in a die-up configuration, in which the bottom package die is carried on the lower surface of the bottom package substrate. ... The die-up flip chip and its flip chip interconnect structures are located within the standoff height of the second-level interconnect structures, and, accordingly, the bottom package die

> in such configurations contributes nothing to the overall thickness of the MPM. Moreover, the die-up configuration can avoid a netlist inversion effect, which typically is a consequence of die-down configuration.

In Maeda JP '326, by contrast, the solder bumps are disposed on the rear surface of the tape board, and the first die is attached on the surface opposite the "rear surface" of the board.

Rejections under 35 U.S.C. § 103(a)

Claims 1 - 5, 11, 12, 17, 35 and 36 were rejected under 35 U.S.C. § 103(a) for obviousness over Halahan U.S. 6,787,916 ("Halahan") in view of Ichinose *et al.* U.S. 6,611,063 ("Ichinose"); Claims 6 - 10, 13 and 19 were rejected under 35 U.S.C. § 103(a) for obviousness over (apparently[1]) Halahan in view of Kakimoto et al. U.S. 6,333,552 ("Kakimoto"); claims 14 - 16 were rejected under 35 U.S.C. § 103(a) for obviousness over Halahan in view of Lin U.S. 5,436,203 ("Lin").These rejections are traversed, at least for the reasons following.

As to claim 1, the Examiner asserted that:

Halahan discloses in e.g., Fig. 1 a multi-package module comprising
- stacked first (166 and 178; column 3, lines 31 and 56) and second packages (108, 104.1 and 104.2; column 2, lines 22-23)
- each said package including a die (178, 104.2 and 104.2) attached to a passive substrate (166 and 108),
- wherein the first (166) and second (108) substrates are interconnected by wire bonding (176; column 3, line 51), and
- wherein the first package (166 and 178) comprises a ball grid array package (see e.g., Fig. 1).

The Examiner acknowledged that "Halahan does not disclose the first package comprising a flip-chip in a die-up configuration." The Examiner asserted that "Ichinose teaches ... a flip-chip (54C; column 7, lines 66 - 67) in a die-up configuration in a package (see Fig. 13)," and argued that it would have been obvious "to add the die of Ichinose et al. at the bottom of the first substrate, opposing the chip 178 of Halahan as taught by Ichinose et al. to increase the performance of the package without increasing the overall thickness of the semiconductor package (abstract, lines 8 - 9)."

[1] The line (item 7., page 5) first asserting the rejection states "unpatentable over Ozawa et al. in view of Kakimoto et al." However, the subsequent detailed reasoning cites Halahan, and it is presumed that the Examiner intended "unpatentable over Halahan in view of Kakimoto et al."

Halahan describes "semiconductor dies ... bonded to contact pads formed in a substrate's cavity" (Abstract). "The substrate can be mounted on a PCB so that the substrate and the PCB enclose the cavity" (Col. 1, lines44 - 46) "The cavity sidewall ... laterally surround the cavity" (Col. 1, lines 50 - 51).

First, generally, an assembly according to Halahan, including interposer 108 and die 104.1, 104.2 cannot be tested before assembly, both because the die 178 on the substrate 166 is not protected and because Halahan does not teach or suggest protecting the die 104.1 and 104.2 prior to assembly. according to Applicant's invention the first and second packages can be tested before they are stacked, so that only packages testing as "good" are used; in the device described by Halahan, there is no testable package.

Applicant does not agree in all particulars with the Examiner's reading of Halahan or of Ichinose. Moreover, it is unclear from the Examiner's articulation how the combination of Halahan with Ichinose is to be made. If the die-up flip-chip die of Ichinose is to be "added" at the bottom opposite the chip 178 of Halahan, is the chip 178 to remain in place in the combination?

Claim 1 is amended herein to recite that the first and second package substrates each have a die attach side and a land side, and the second package is stacked over the first package such that a portion of the land side of the second package opposite the second package die is affixed to a surface of the first package. This clearly distinguishes the configurations described in Halahan, inasmuch as the interposer 108 of Halahan has a cavity where the second package die are attached, so that the interposer 108 cannot be affixed to a surface of the first package and instead must necessarily be attached to the first package substrate by a peripheral portion. Neither Halahan nor Ichinose, nor any combination of them, teaches or suggests Applicant's invention as claimed in claim 1 as amended and, accordingly, the rejection of claim 1 (and claims depending from it) over Halahan in combination with Ichinose should be withdrawn.

As to claims 6 - 10, 13 and 19, The Examiner asserted that "Halahan discloses in e.g., Fig. 1 the second package being stacked over the first package (claim 13) and the use of a chip in a flip chip package;" then the Examiner acknowledges that "Halahan does not appear to provide a specific type of the die t be an RF die (claim 8) and an electrical shield (claims 6, 10 and 13) in the package; Kakimoto is relied upon (with reference to Kakimoto Figs. 6 and 7) as describing an electrical shield and an RF die in a flip chip package. As noted above, Ozawa fails to suggest or describe a multi-package module having stacked packages and, as there is no suggestion in

Kakimoto of stacked packages, Kakimoto cannot supply what Ozawa lacks. Accordingly, no combination of Kakimoto with Ozawa makes Applicant's claimed invention, and the rejection of claims 6 - 10, 13 and 19 for obviousness over Halahan in view of Kakimoto should be withdrawn.

As to claims 14 - 16, the Examiner acknowledged that Halahan "does not appear to provide an embedded ground plane in the first package substrate"; Lin is relied upon (with reference to Lin Fig. 1) as describing an embedded ground plane in a package substrate. As the Examiner acknowledged in the rejections over Halahan in view of Ichinose, Halahan also fails to describe the first package comprising a flip-chip BGA package having a flip chip in a die-up configuration, as recited in Applicant's claims, and this feature is not supplied by Lin. Accordingly, the asserted combination does not make Applicant's invention as claimed, and the rejection of claims 14 - 16 for obviousness over Halahan in view of Lin should be withdrawn.

In view of the foregoing, all the claims now in the application are believed to be in condition for allowance, and action to that effect is respectfully requested

This Amendment is being filed within the second month following the three-months; shortened statutory period set by the Examiner for response and, accordingly, it is accompanied by a petition for two months' extension of time and a fee or fee authorization therefor. In the event the Examiner may determine that a further extension of time may be required in connection with the filing of this paper, petition is hereby made therefor, and the Commissioner is authorized to charge any additional fee (or to credit any overpayment) to Deposit Account No. 50-0869 (CPAC 1017-5).

If the Examiner determines that a conference would facilitate prosecution of this application, the Examiner is invited to telephone Applicants' representative, undersigned, at the telephone number set out below.

Respectfully submitted,

Reg. No. 33,407

Bill Kennedy
Reg. No. 33,407

Haynes Beffel & Wolfeld LLP
P.O. Box 366
Half Moon Bay, CA 94019
Telephone: (650) 712-0340